REMARKS

This AMENDMENT UNDER 37 CFR 1.111 is filed in reply to the outstanding Office Action of October 6, 2003, and is believed to place this case in condition for allowance for reasons set forth below in greater detail.

Responsive to paragraphs 1-3 of the Office Action:

proposed annotated sheets showing changes to Figures 1A, 1B, 1C(1), 1C(2), and 3 are attached hereto, and the changes are explained in detail in Amendments to the Drawings.

the specification has been amended in Amendments to the Specification to add paragraphs which explain all reference characters and dimensions shown in the drawings, all of which are believed to be fully supported by the original specification without any issues of new matter. The paragraph on page 7, lines 8-19, has been corrected to refer to read operations R, as was done previously for read R3' in that same paragraph.

Responsive to paragraph 4, the noted correction has been made to claim 6.

Responsive to paragraph 6, the operation of the circuit of Figure 1A is quite simple, and would be readily apparent to one skilled in this art.

The following explanation is for the operation of the first pair of nMOS transfer devices N5, N6, controlled by wordline W1 and connected respectively to the bitlines B1, BB1. The operation of the second pair of nMOS transfer devices N3, N4 is analogously parallel, only with N3, N4 controlled by the wordline W2 and connected respectively to the bitlines B2, BB2.

The explanation of Figure 1A spanning pages 3 and 4 states "A first pair of transfer nMOS devices N5 and N6 allow the internal nodes N to be accessed by the first pair

of the bit-lines, B1 and BB1...A first wordline W1 is connected to the gates of the first pair nMOS transfer devices N5, N6 (to turn on or off the first pair of transfer devices N5, N6).

This explanation implies and requires that the Vdd voltage supply is applied, via the bitlines B1, BB1, when the devices N5, N6 are turned on.

The explanation at page 4, lines 6-8, states, "When the cell is not selected, both wordlines W1 and W2 are held "low" to turn off the nMOS devices N3, N4, N5 and N6. The off-state current (leakage current) serves to replenish the charge stored in the storage nodes N." A leakage current requires and implies that a voltage Vdd is applied to the devices N5, N6, via the bitlines B1, BB1, when the devices N5 and N6 are off, to produce the leakage current. And, in fact, the application of such a pre-charge voltage to the bitlines prior to activation is exactly the way prior art SRAM cells operate, which include two pull-up pMOS devices - unlike the present invention which advantageously has six nMOS devices and no PMOS devices.

The explanation at page 4, lines 10-12, continues, "At any one moment, only one wordline in a row is activated. Therefore, for the selected cells, there will always be a pair of pull-up devices to provide a constant load to the cells." For operation of the first pair of devices N5 and N6, this means wordline W1 is activated, and the second pair of devices N3, N4 "provide a constant load" and act as pull-up devices.

In summary of the above explanations in the specification:

(1) At all times without read or write operations, all of the wordlines are off, and all the bitlines are connected to precharge Vdd (Power Supply), similar to and as is known in the prior art.

(2) During a write operation, if W1 is activated, the corresponding bitline pair, B1 and BB1 provide differential signals ("1" and "0"), W2 is off, and N3 and N4 are the loading devices, acting like pull-up resistors.

(3) During a read operation, if W1 is activated, the corresponding bitline pair B1 and BB1 are floating, W2 is off, and N3 and N4 are the loading devices, acting like pull-up resistors.

The above operation is very analogous to operation of prior art SRAM cells and would be apparent to one skilled in this art, with the major exception that the present invention very advantageously does not include pull-up pMOS devices as in the prior art.

Reconsideration is respectfully requested of the rejection of the claims herein over Lattimore et al, particularly in view of the distinguishing amendments to independent claims 1 and 6, and the following comments on the advantages and distinctions of the present invention relative to Lattimore et al.

Claims 2 and 3 have been cancelled as their limitations are now in claim 1.

Claims 13 and 14 have been added to further distinguish over Lattimore et al., and recite the closed end limitation "composed of." Claim 13 distinguishes over the four bitlines of Lattimore, and claim 14 distinguishes over the four transfer devices of Lattimore.

Lattimore discloses an SRAM memory cell having

nMOS pull-down devices N1, N2,

pMOS pull-up devices P1, P2, and

nMOS transfer devices N4/N6, N3/N5.

The present invention advantageously distinguishes over Lattimore by using no pMOS pull-up devices, and instead using, as recited by claim 1, a first pair of nMOS transfer

devices, and a second pair of nMOS transfer devices, wherein, when one pair of nMOS transfer devices is activated by its coupled wordline, the other pair of nMOS transfer devices functions as load pull-up devices.

The dual port SRAM cell of the present invention advantageously uses only six nMOS devices, which presents significant advantages as explained in the specification.

Lattimore et al only discloses a single dual port memory cell which is not capable of the interleaved memory operations of the present invention.

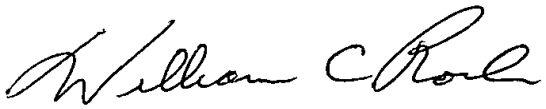
Independent claim 6 covers the asymmetrical memory cell circuit design of Figure 1B for a dual port SRAM cell having only four nMOS and three pMOS devices,

first and second nMOS pull-down devices,
first and second pMOS pull-up devices,
first and second nMOS transfer devices, and
a single pMOS transfer device, having
first and second bitlines coupled respectively to the drains of the first and second nMOS transfer devices,
a third bitline coupled to the drain of the single pMOS transfer device,
a first wordline coupled to the gates of the first and second nMOS transfer devices, and
a second wordline coupled to the gate of the single pMOS transfer device.

In contrast to the circuit of independent claim 6, the Lattimore et al memory cell comprises four nMOS transfer devices, and so does not anticipate or render obvious the subject matter of claim 6.

This application is now believed to be in condition for allowance, a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,



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Enclosures